What is claimed is:

[c1] 1.A rings-based system on a chip, comprising:
a plurality of ring members on a ring that communicate using point-to-point connectivity;
a message traversing the ring from member to member;
the system being adapted so that upon the message arriving at a given ring member the message is processed by that member if the message is applicable to that ring member, and if the message is not applicable to that ring member, the message is passed on to the next ring member;
the system being adapted to process both read messages and write messages;
the plurality of ring members including a CPU and at least one peripheral that exchanges date with the CPU;
wherein the peripheral includes at least one status memory that stores data describing the status of the peripheral;
and wherein the system is configured to write ahead status changes that are accessible by the CPU.

[c2] 2.The system of claim 1, wherein the status memory comprises at least one status register.

[c3] 3.The system of claim 1, wherein the system is adapted to perform write ahead status changes that would otherwise be initiated by the CPU as read operations.

[c4] 4.The system of claim 1, wherein the system is adapted to write ahead status changes to a RAM on the CPU or a RAM that is accessible by the CPU.

[c5] 5.The system of claim 1, wherein the write ahead operations are performed for some peripheral status changes but not other peripheral status changes.

[c6] 6.The system of claim 5, wherein the write ahead operation is performed or not performed depending on the nature of the status change.

[c7] 7.The system of claim 5, wherein the write ahead operation is performed or not performed based on the magnitude or the quantity of the status change.

[c8] 8.The system of claim 1, wherein the write ahead operations are programmed to

occur based on read operations that would otherwise be initiated by the CPU on a regular basis.

[c9] 9.The system of claim 1, wherein the CPU comprises a control protocol processor in a communications chip.

[c10] 10.The system of claim 1, wherein the CPU comprises a network processor in a communications chip.

[c11] 11.A method for processing in a rings based communication system, comprising:
identifying at least one module in a ring network that includes status registers that store status information of regular interest to a processor in the ring network;
identifying which status information can be transmitted to the processor as a write ahead operation initiated by the at least one module instead of a read operation initiated by the processing;
programming the at least one module to transmit the identified status information as a write ahead operation.

[c12] 12.The method of claim 11, wherein the identification comprises identifying which status changes are of critical importance or of regular interest to the processor.

[c13] 13.The method of claim 11, wherein the identification includes identifying what magnitude or level of status change will cause the write ahead operation.

[c14] 14.The method of claim 11, wherein the step of programming causes the average number of read operations initiated by the processor to decrease.

[c15] 15.The method of claim 11, wherein the processor comprises a protocol processor or a network processor.